CSE 2600
Intro. To Digital Logic & Computer Design

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&
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Reminder

- Studios can (and should) be done collaboratively!
- Homework should be done *independently*
  - Ok to discuss *ideas* and related work from *studio*
  - Should not discuss / share details of specific solutions

This week & misc.

- Hw #3B Posted / Due Sunday
- Almost done assigning all remaining studio prep sessions. Expect to send out details Wednesday

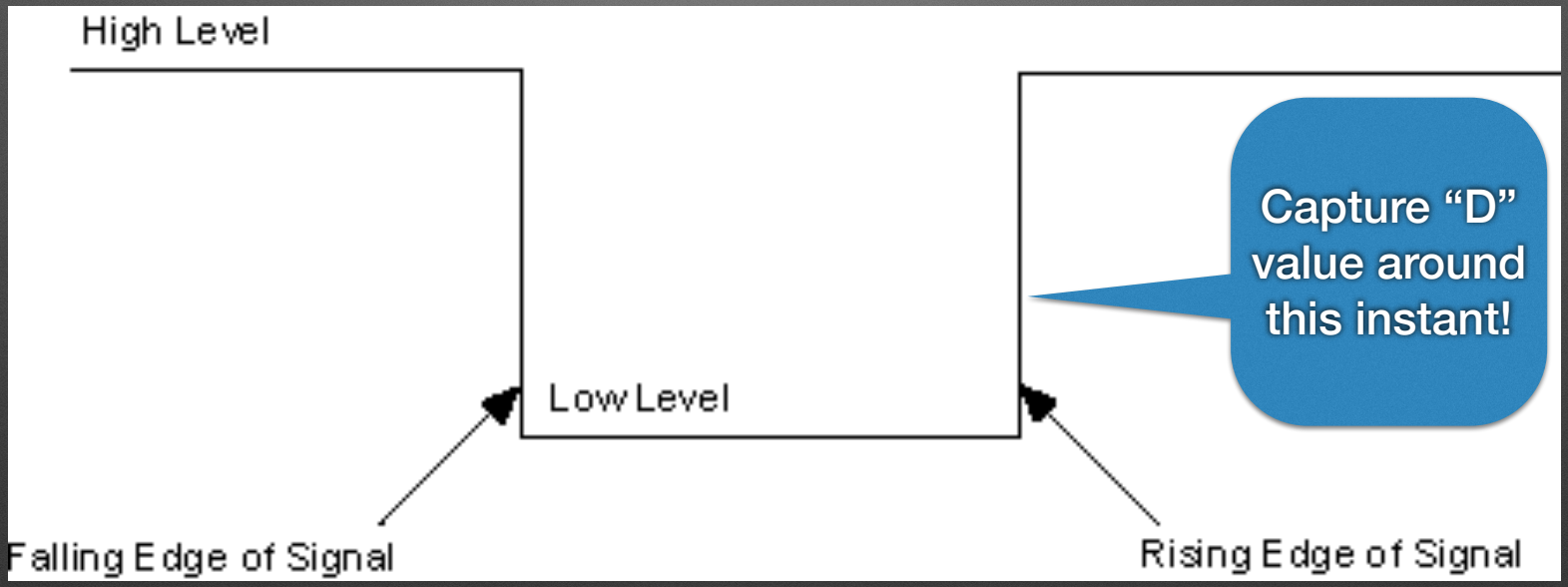
Last Lecture

- Sequential Circuits: Have a loop and outputs impact the inputs
- Bistable: Will hold one of two different states
  - May have some “metastable” condition (oscillating or between 1/0)
- SR-Latch: Cross-coupled NOR version
  - JLS version & time
  - Racing and unpredictable behavior

SR Latch Issues: Hazardous Conditions!

- Short pulse
- R & S dropping at the same time

D-Flip-Flop Clock



https://www.ni.com/docs/en-US/bundle/ni-hsdio/page/hsdio/fedge_trigger.html

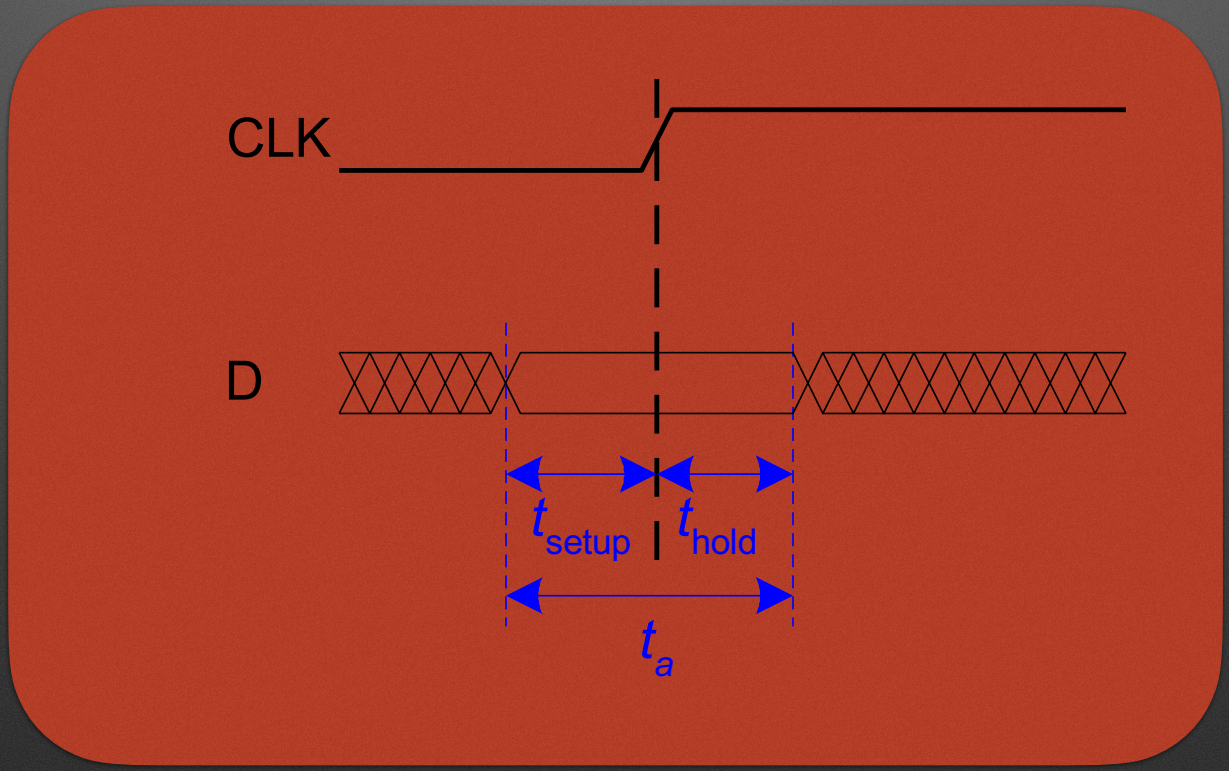
Last Lecture

- D Latch: Transparent on high clock
- D Flip-Flop: Two D-latches that are transparent at opposite clock levels
  - Provide precise timing of data *acquisition* / storage
  - General focus: positive/rising edge triggers

D Flip Flop can be built from SR Latches

- Internal latch
  - Fails if pulses too short
  - Unstable if R/S drop at same time / too close
- Setup Time: Time needed before clock to ensure stable capture
- Hold Time: Time After clock edge value must be “held”

Dff: Setup & Hold Time

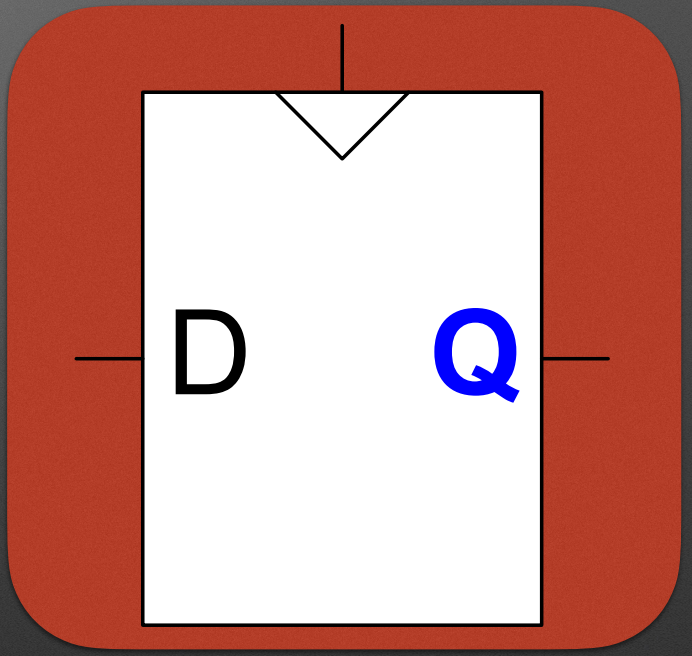


D Flip Flop Time Parameters

- t_{setup}: Time D must be stable before clock
- t_{hold}: Time D must be stable after clock
- t_a: Aperture time ($t_{setup} + t_{hold}$) –
  total window of time D needs to be stable around clock

Dff Time Parameters *Relative to Clock*

- t_{pcq}: Propagation delay from Clock to Q (pcq)
- t_{ccq}: Contamination delay from C to Q (ccq)



Sequential & Synchronous Logic

- *Sequential* circuits
  - Can’t be represented with a *simple* table of just inputs and outputs (Possibly a complex table of history of inputs and outputs)
  - Output depends on sequence of inputs and timing
  - *Synchronous* Sequential Circuits
    - Sequential circuits with additional restrictions on form to improve predictability

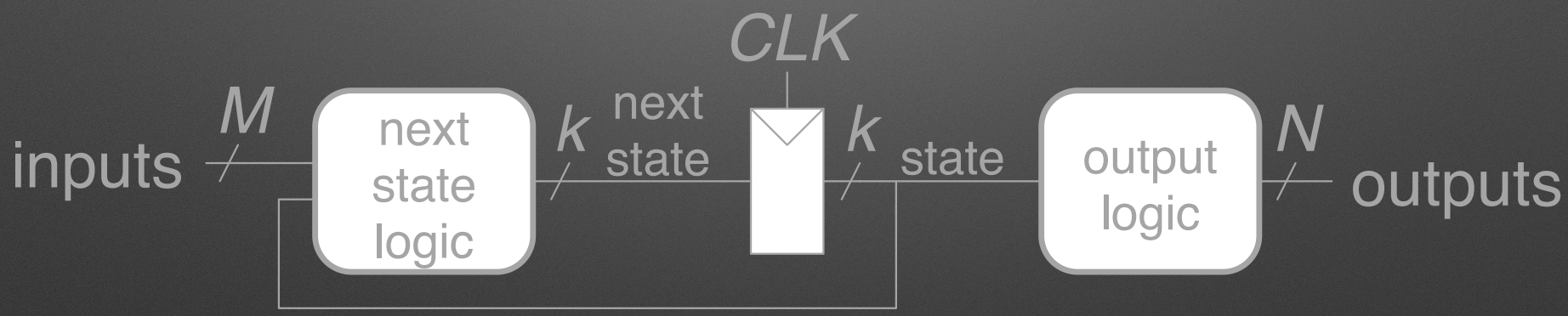
Synchronous Sequential Circuits

- Are *synchronized* by a common clock
- Uses registers (*D Flip-Flops*)
- Mix of registers and combinational logic
- All cycles in circuit include *at least one register*
- Goal: Impose predictable behavior!

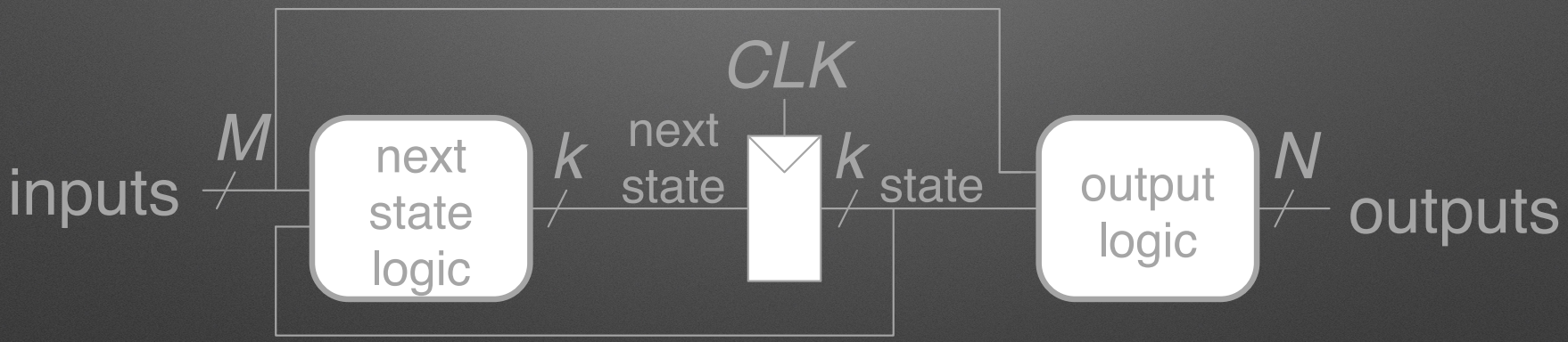
Finite State Machines

- Can be realized with *synchronous* sequential circuits
  - Memory (registers/flip-flops) hold *encoded* state (represents the location or current bubble in diagram)
  - Combinational logic for:
    - Output control (the outputs in the bubbles)
    - Determine next state (the arrows)

FSM: Moore Machine Structure



FSM: Mealy Machine



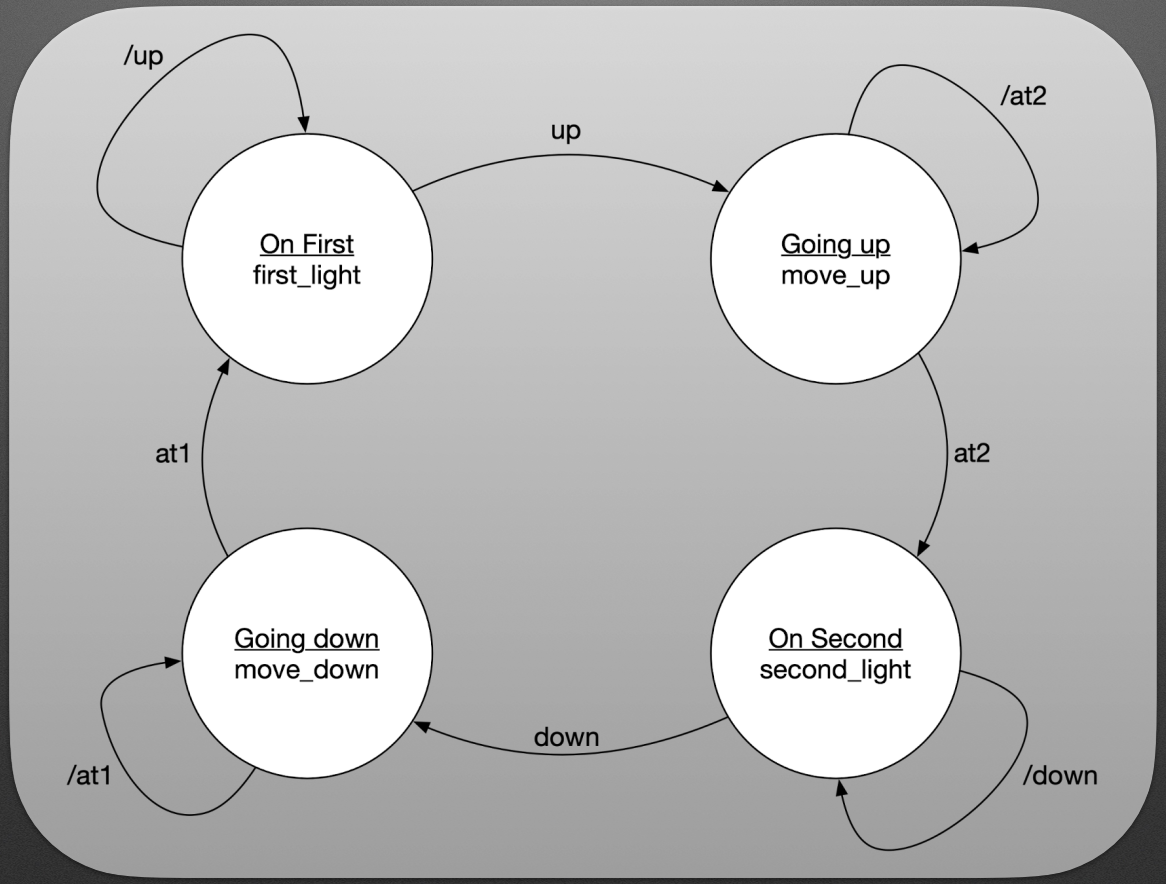
FSM Applications

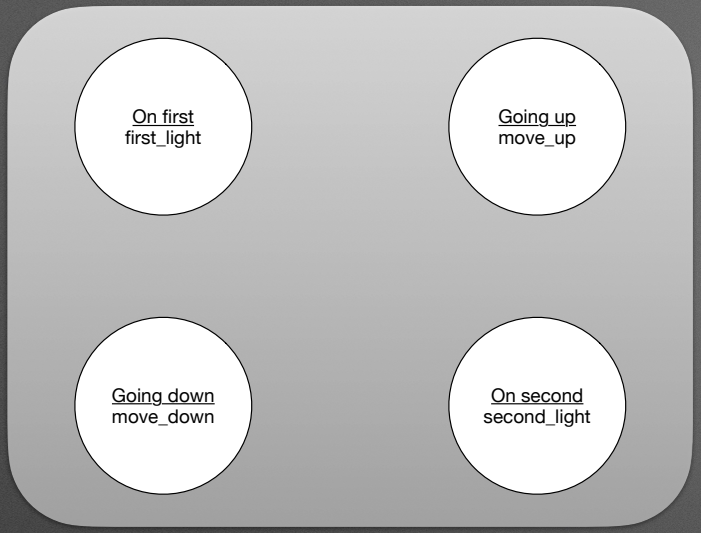
- Things with modes or sequences of steps. Examples:
  - Washing Machine (fill, agitate, rinse, spin)
  - Stop lights & Traffic control: Green, Yellow, Red
  - Locks: Locked & unlocked
  - Computer programs: Playing game vs. on menu
  - Elevator controls (state = floor)
  - …

Studio 3A Summary

- 74F175: Memory/storage, bits, and resets
- Elevator Example

Overall


/up
up
/at2
On First
first_light
Going up
move_up
at1
at2
Going down
move_down
On Second
second_light
down
/at1
/down



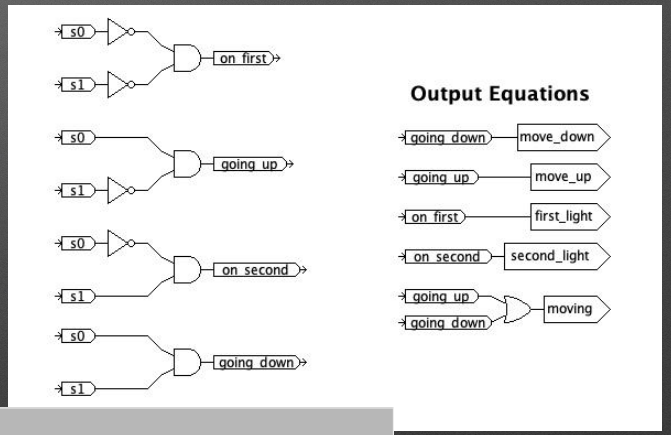
Overall

State Encoding

State Name	Numeric Encoding	State Bits	
		S1	S0
On first	0	0	0
Going up	1	0	1
On second	2	1	0
Going	3	1	1

Output Equations

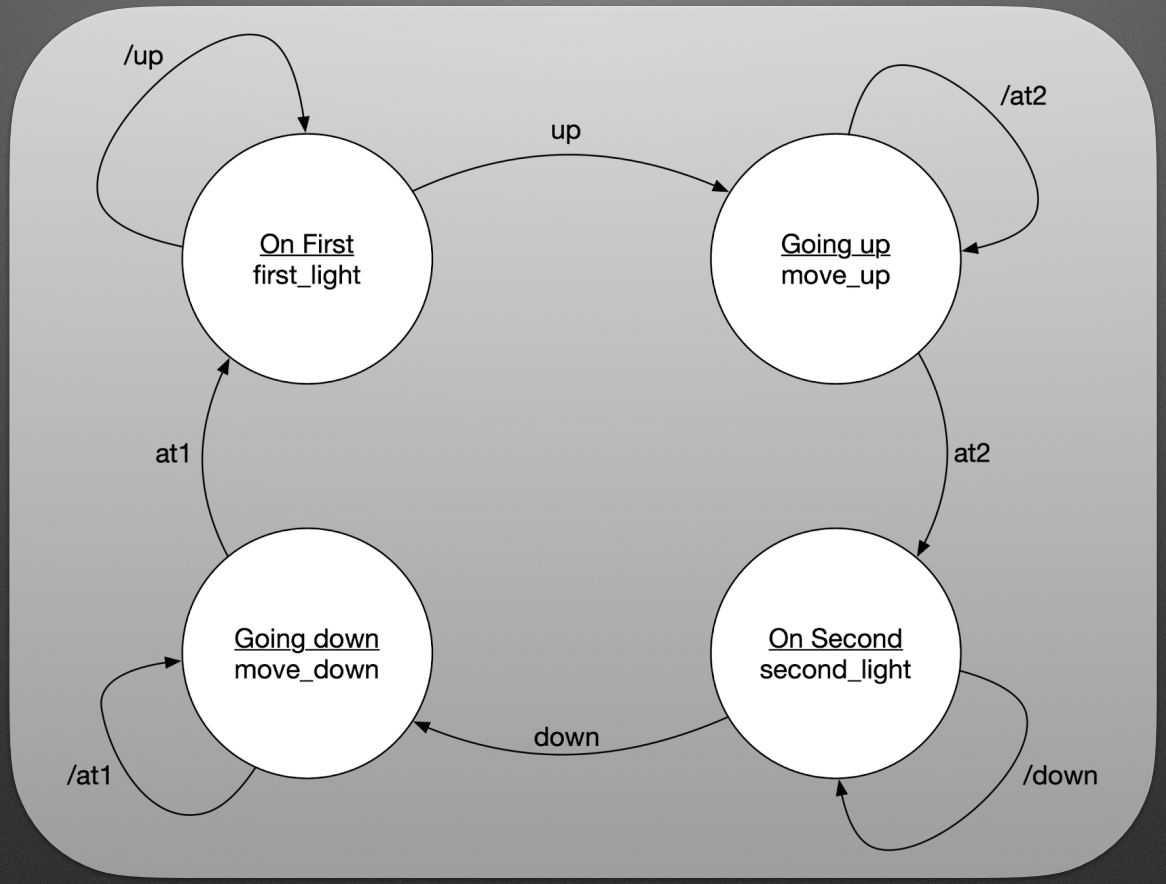
move_up = Going_up = /S1*S0
move_down = Going_down = S1*S0
first_light = On_First =/S1*/S0
second_light =On_Second = S1*/S0
moving = Going_up + Going_down = /S1*S0 + S1*S0

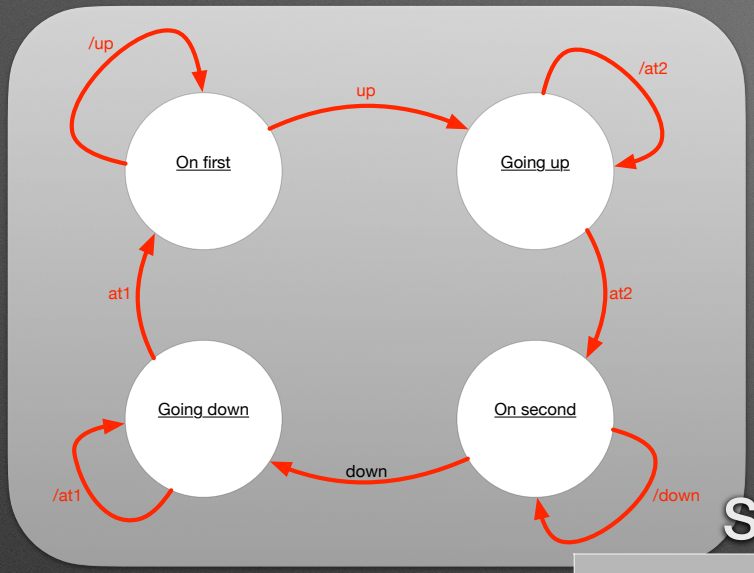


Output Decisions (based on state)

State Name	Numeric Encoding	State Bits		Outputs				
		S1	S0	move_up	move_down	first_light	second_light	moving
On first	0	0	0	0	0	1	0	0
Going up	1	0	1	1	0	0	0	1
On second	2	1	0	0	0	0	1	0
Going down	3	1	1	0	1	0	0	1

Overall


/up
up
/at2
On First
first_light
Going up
move_up
at1
at2
Going down
move_down
On Second
second_light
down
/at1
/down



Overall

State Encoding

State Name	Numeric Encoding	State Bits	
		S1	S0
On first	0	0	0
Going up	1	0	1
On second	2	1	0
Going	3	1	1

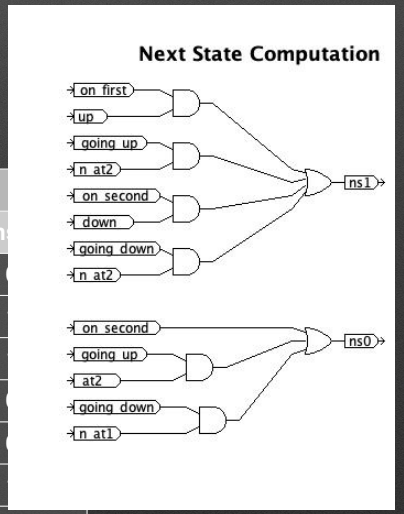
Next State Equations

ns1 = On_Second*at2 +
On_second*/down +
Going_down*down +
Going_down*/at1

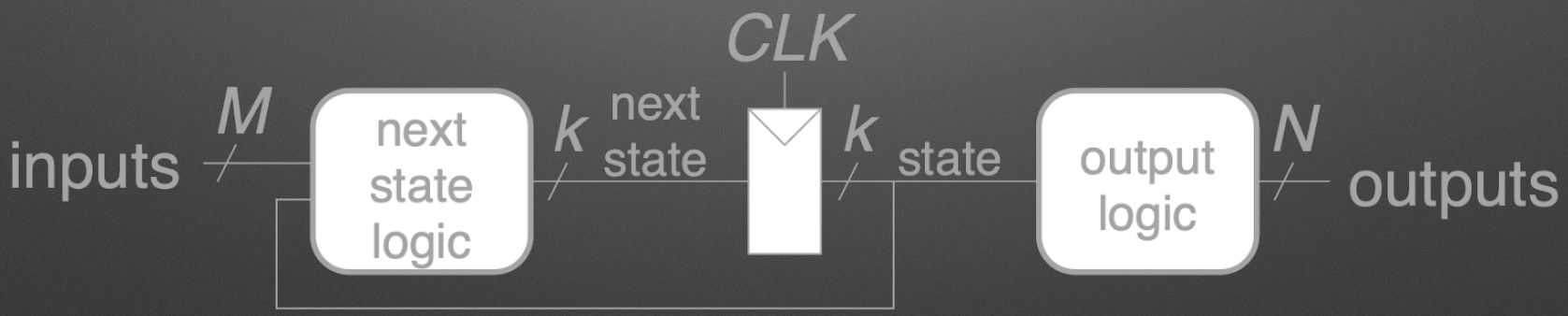
ns0 = Going_up*up +
Going_up*/at2 +
On_second*down +
Going_down*/at1

State Transitions (to "next state")

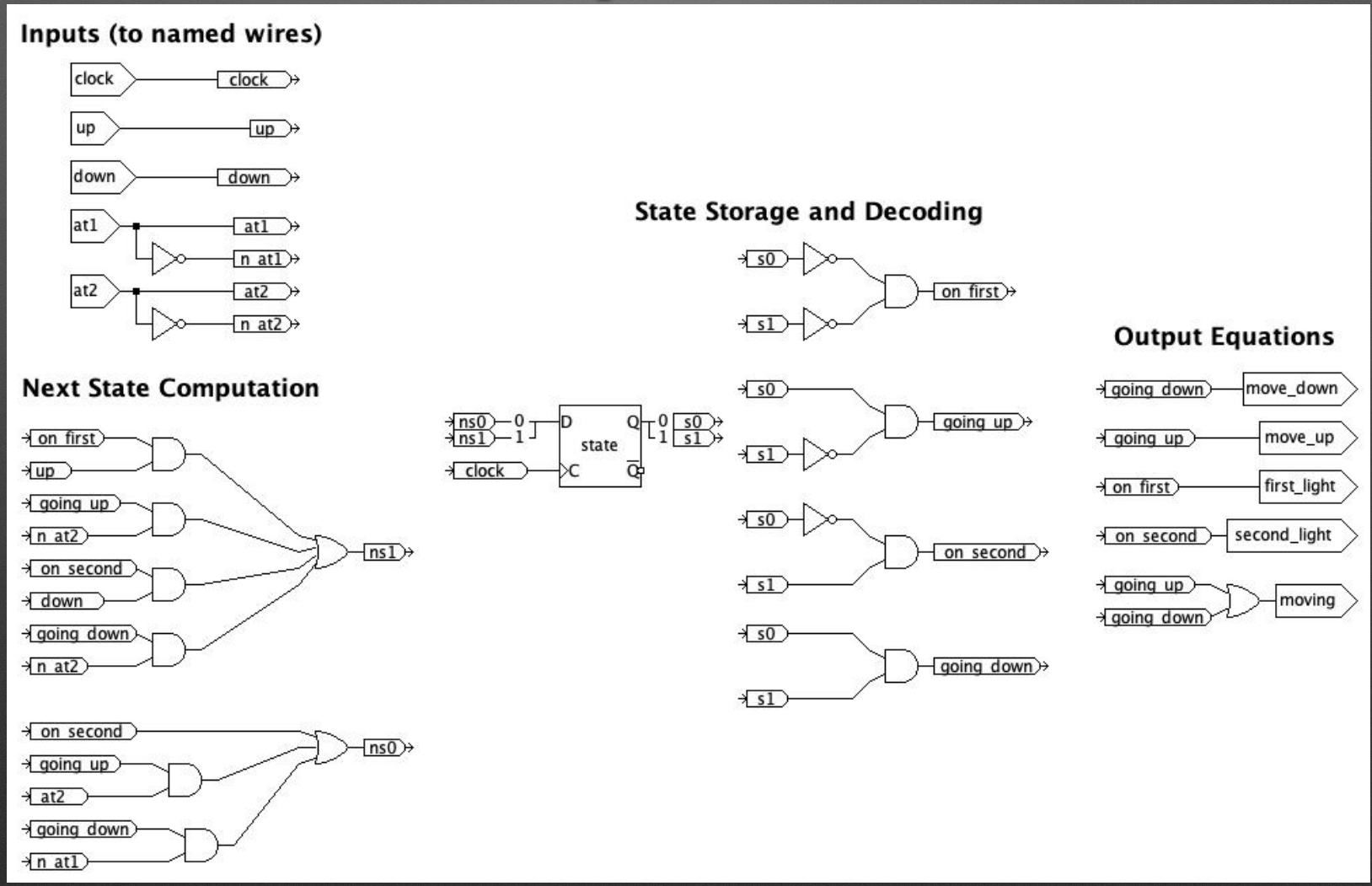
State Name	Numeric Encoding	Inputs				Next State		
		up	down	at1	at2	Name	ns1	n
On first	0	0	X	X	X	On_first	0	
		1	X	X	X	Going_up	0	
Going up	1	X	X	X	0	Going_up	0	
		X	X	X	1	On_second	1	
On second	2	X	0	X	X	On_second	1	
		X	1	X	X	Going_down	1	
Going down	3	X	X	0	X	Going_down	1	1
		X	X	1	X	On_first	0	0



Overall Structure



Overall Implementation



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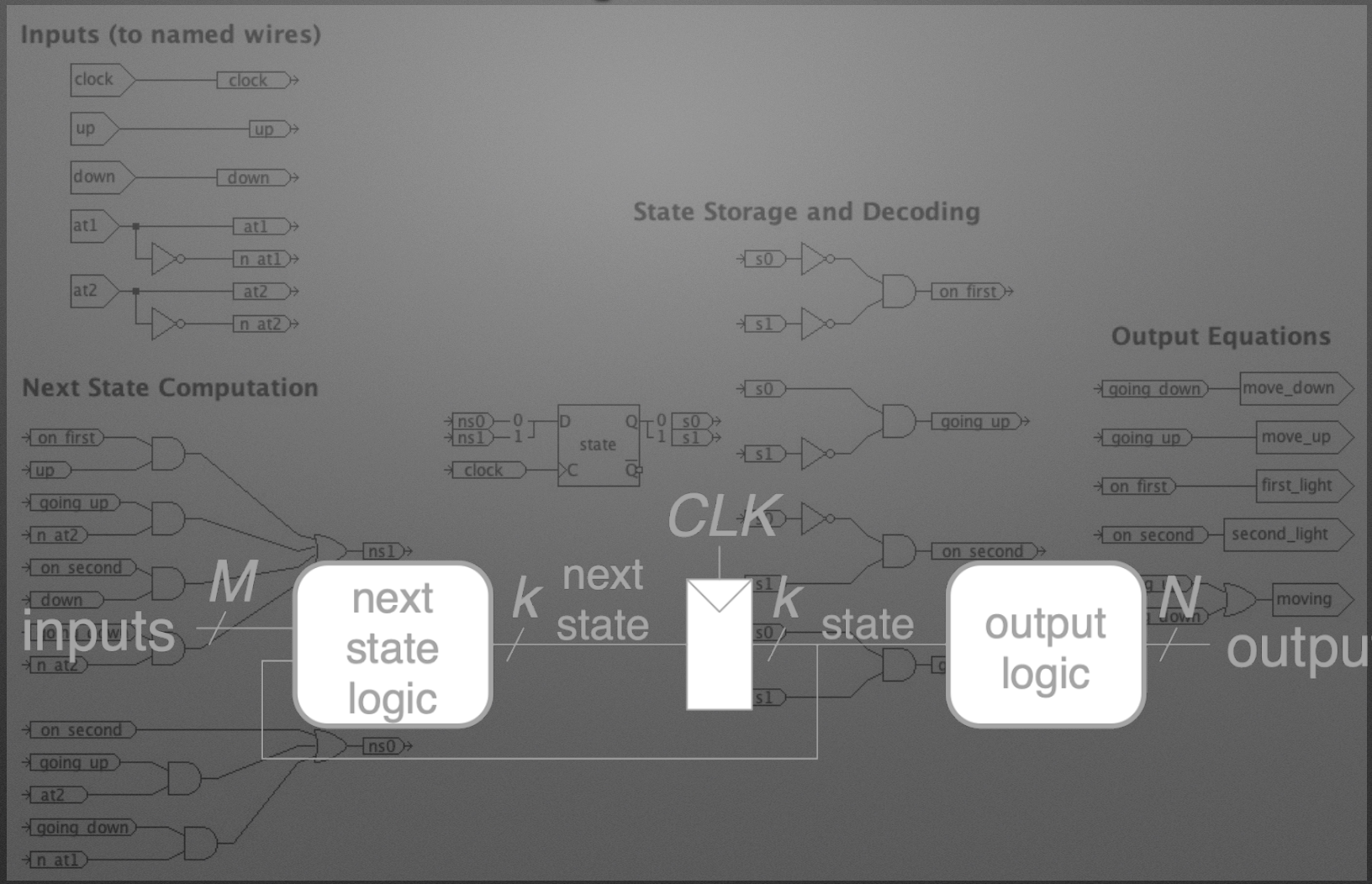
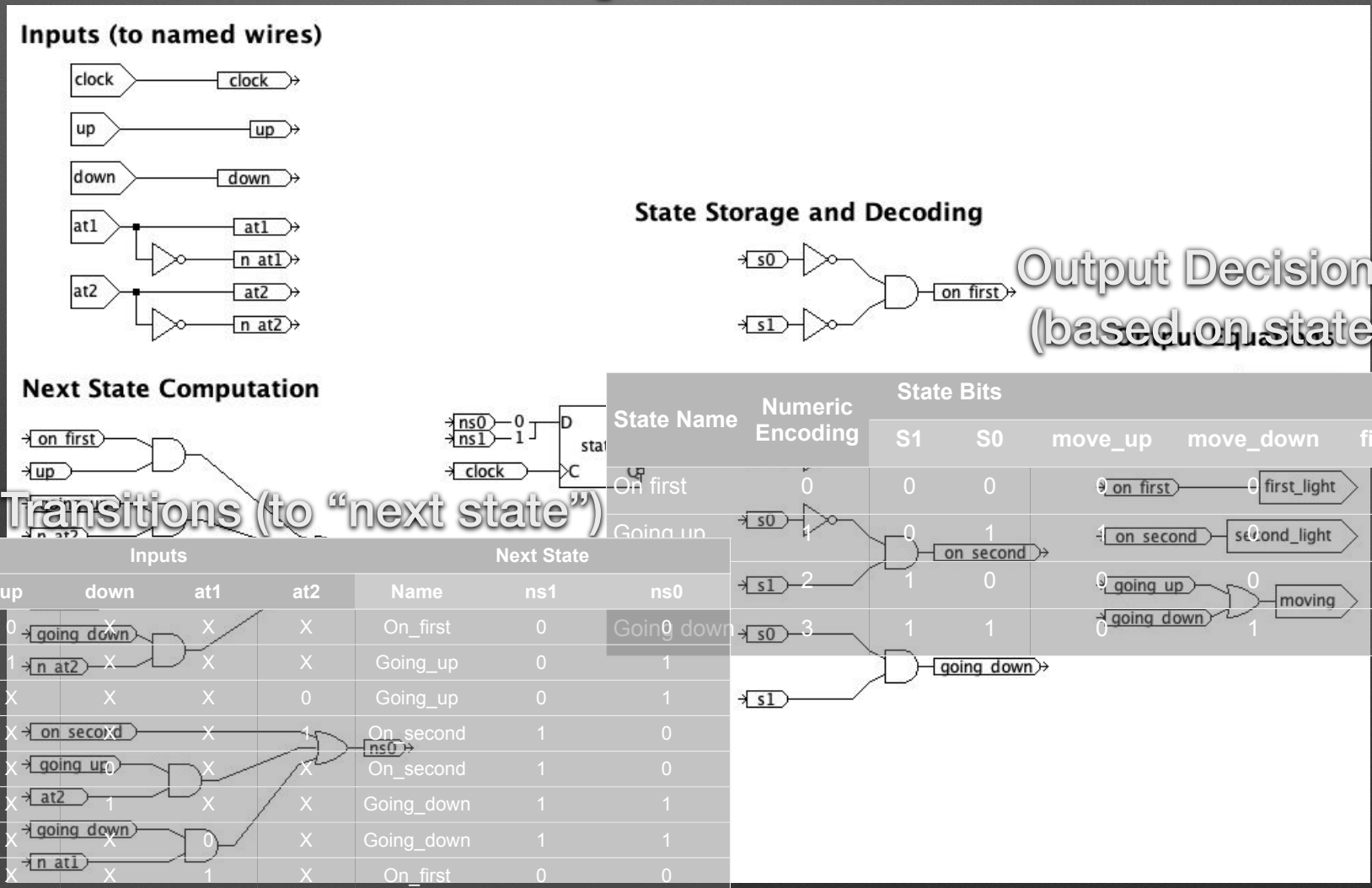


Overall Implementation



State Transitions (to "next state")

State Name	Numeric Encoding	Inputs				Next State		
		up	down	at1	at2	Name	ns1	ns0
On first	0	0	X	X	X	On_first	0	0
		1	X	X	X	Going_up	0	1
Going up	1	X	X	X	0	Going_up	0	1
		X	X	X	1	On_second	1	0
On second	2	X	X	X	X	On_second	1	0
		X	1	X	X	Going_down	1	1
Going down	3	X	X	0	X	Going_down	1	1
		X	X	1	X	On_first	0	0

Output Decisions (based on state)

State Name	Numeric Encoding	State Bits		Outputs			
		S1	S0	move_up	move_down	first_light	sec
On first	0	0	0	0	0	1	
Going up	1	0	1	1	0	0	
On second	2	1	0	0	0	0	
Going down	3	1	1	0	1	0	

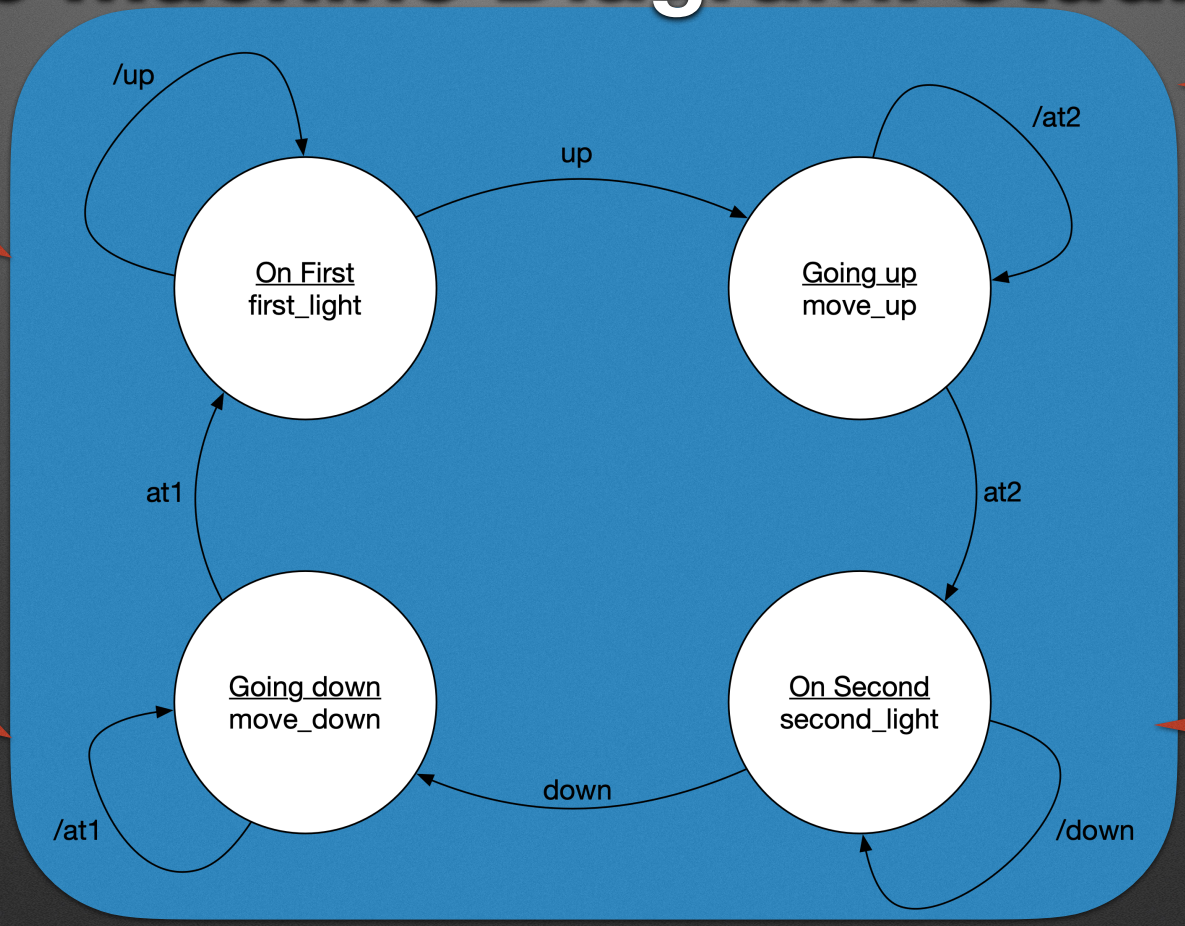
e Machine Diagram: Studic

Assume clock cycle of 10s?

Vs 240s?

What does “clock” do?

Can the clock be too short?



State Encodings

- “Art”
  - Encoding has impact on equations used
- Major flavors
  - Counting
  - One Hot

Elevator: Examples

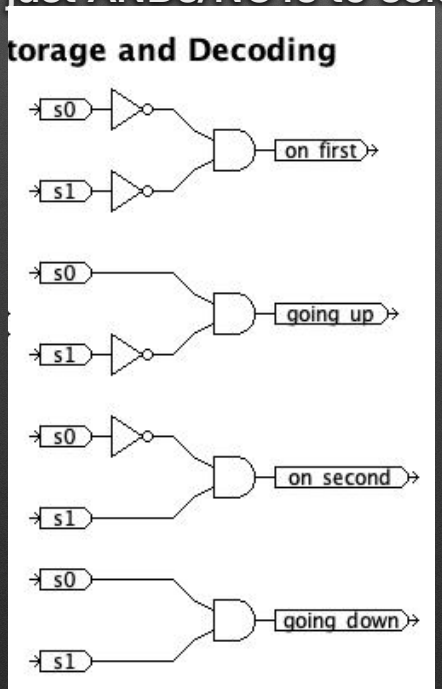
STATE NAME	BINARY COUNTING	ONE HOT
ON FIRST		
GOING UP		
ON SECOND		
GOING DOWN		

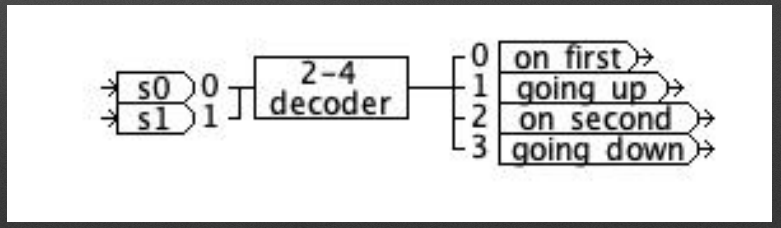
Elevator: Examples Part 2

STATE NAME	BINARY COUNTING	ONE HOT
ON FIRST		
GOING UP		
ON SECOND		
GOING DOWN		

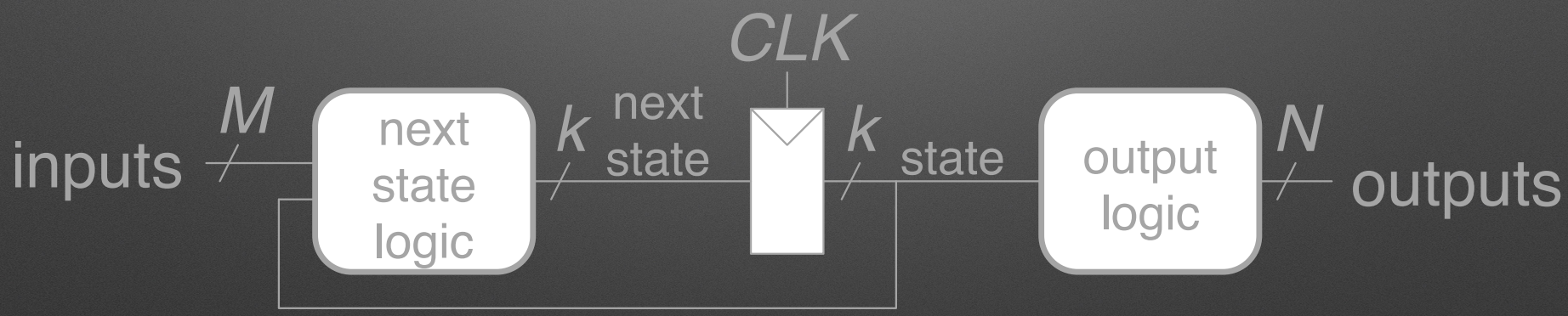
Decoder

- Decoders…decode
  - n bits of input to 2^n distinct, mutually exclusive outputs
  - It's just ANDs/NOTs to select each distinct binary value





Review: Moore Machine Structure



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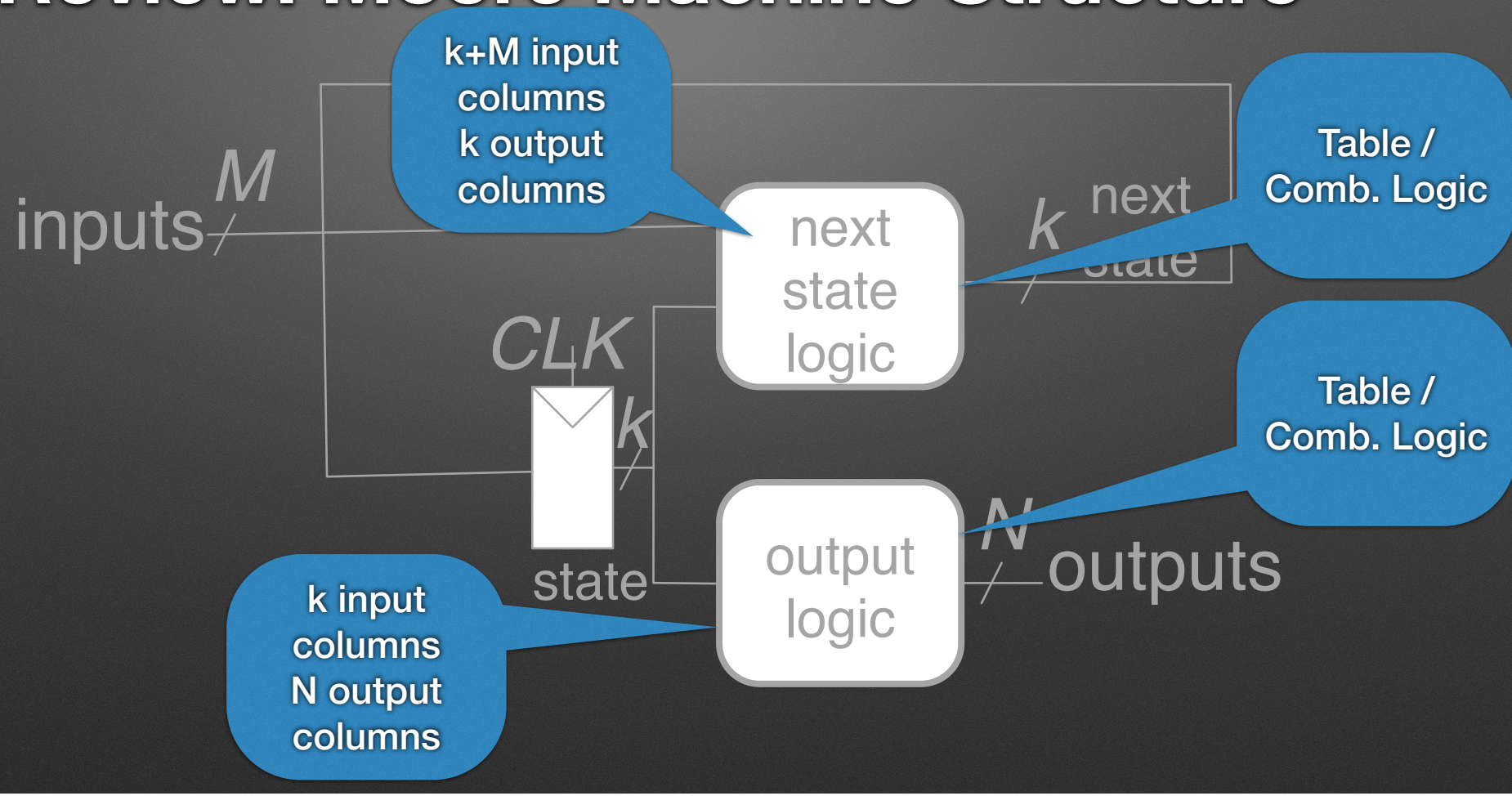
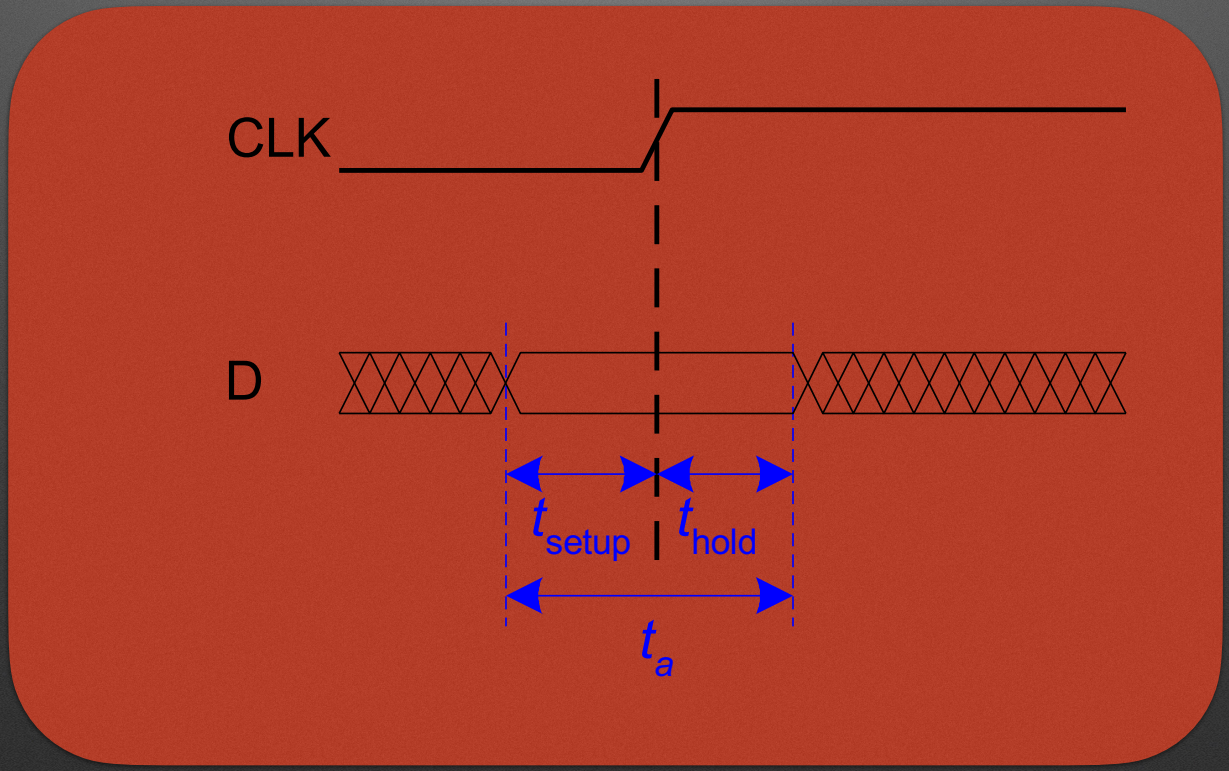
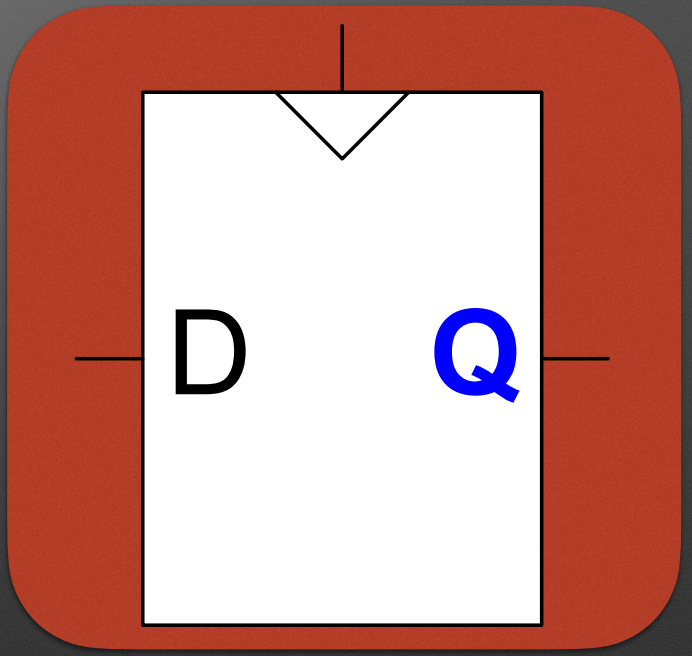


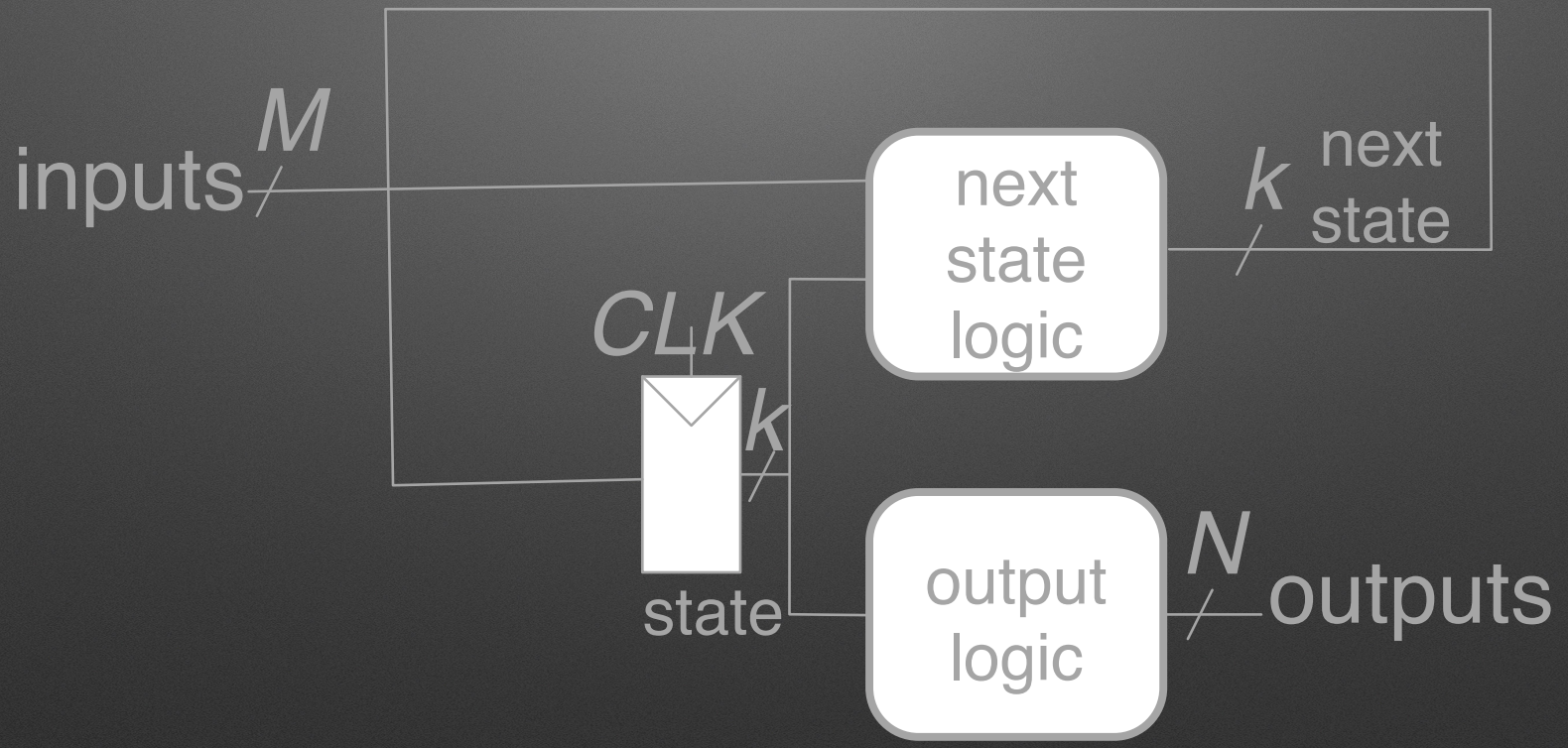
Review: Dff Setup & Hold Time



Dff Time Parameters

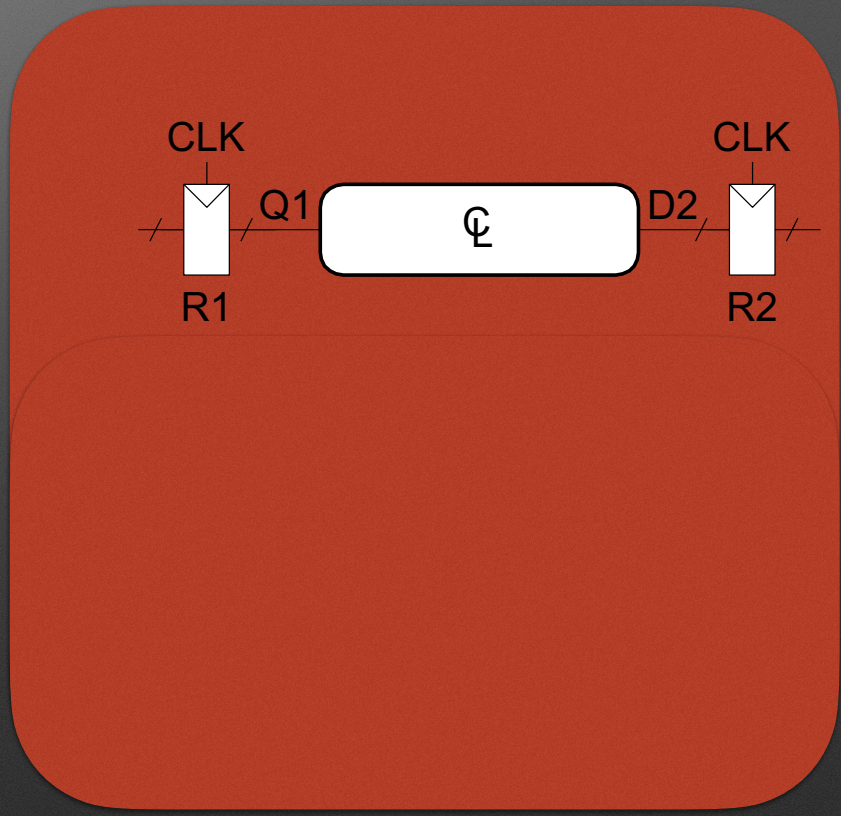
- t_{pcq}: Propagation delay from Clock to Q (pcq)
- t_{ccq}: Contamination delay from C to Q (ccq)




inputs
M
next
state
logic
k
next
state
CLK
k
state
output
logic
N
outputs

Setup Time Constraint

- Max time from R1 through CL
  - R2's input needs to be stable t_{setup} before clock



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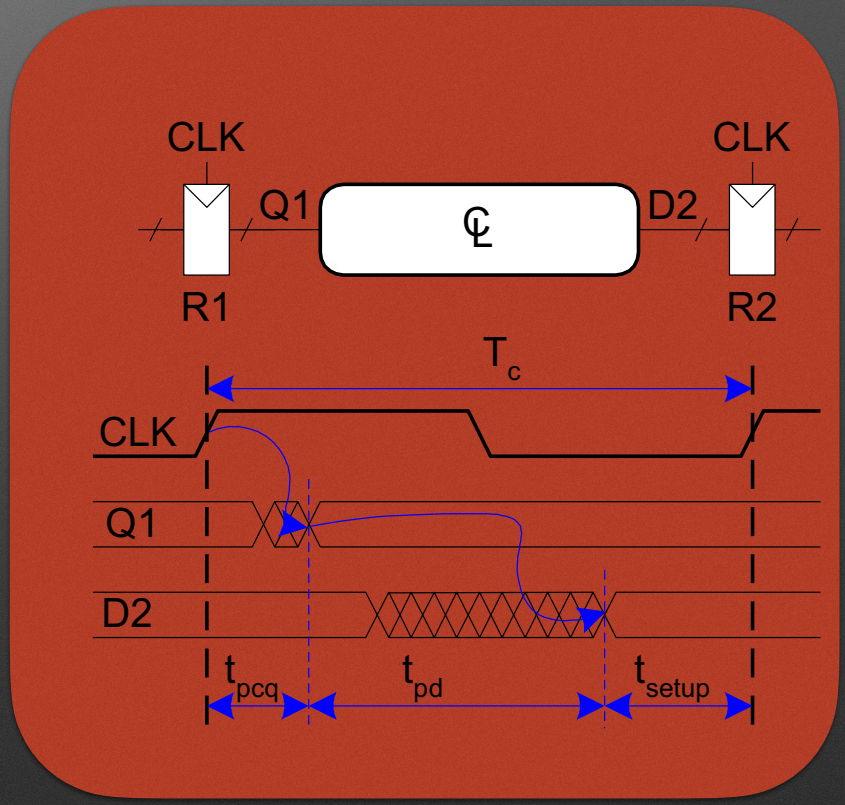
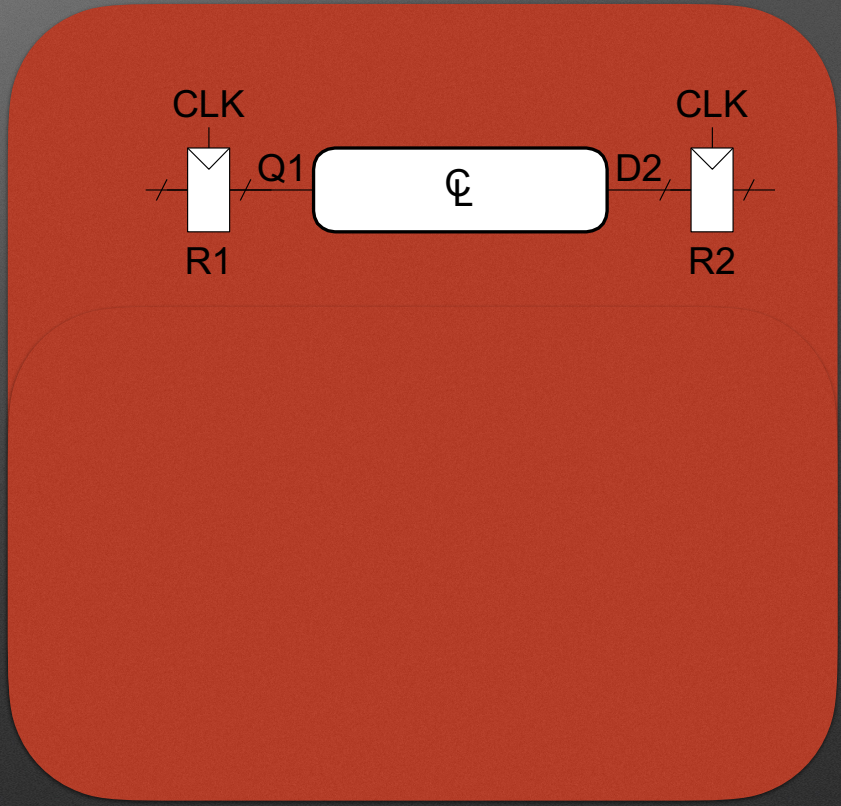


Hold Time Constraint

- Min time from R1 through CL
  - R2's input must be stable t_{hold} after the clock



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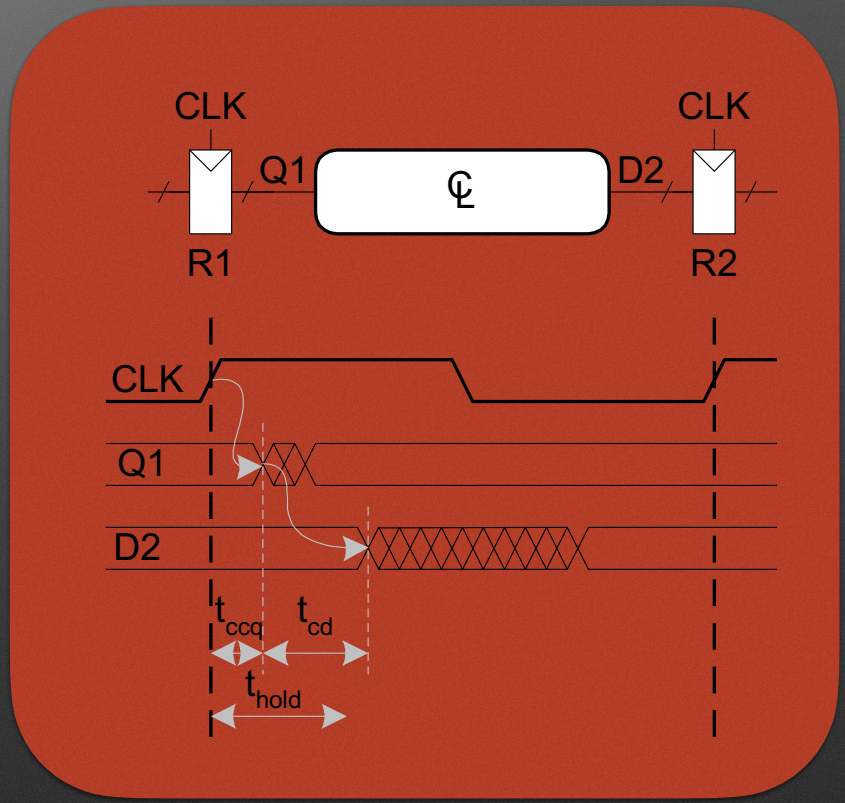
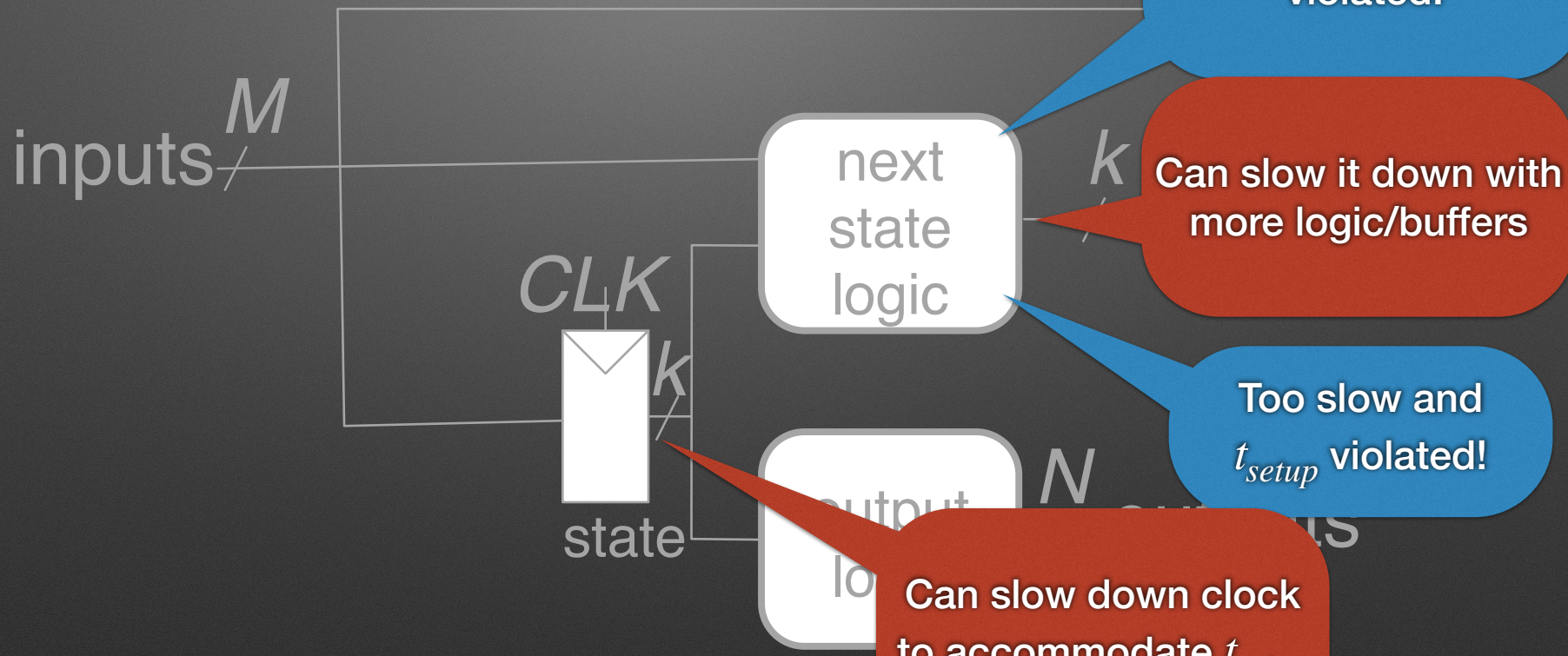
- Min time from R1 through CL
  - R2's input must be stable t_{hold} after the clock



Review: Moore Machine Stru



Synchronous Timing

- Must meet both
  - Setup Time Constraint
  - Hold Time Constraint

Next Time

- Studio