CSE 2600 - Homework 2A

Always show all work for full credit.

1. Review: Fill in the missing values in the following table (all values are unsigned)

Binary	Decimal	Hex
1110100		
		0x1CA
	268	

2. Write a Boolean equation in sum-of-products canonical form for:

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

3. Write a Boolean equation in sum-of-products canonical form for:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

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4. Write a Boolean equation in sum-of-products canonical form for:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

5. Write a Boolean equation in sum-of-products canonical form for:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

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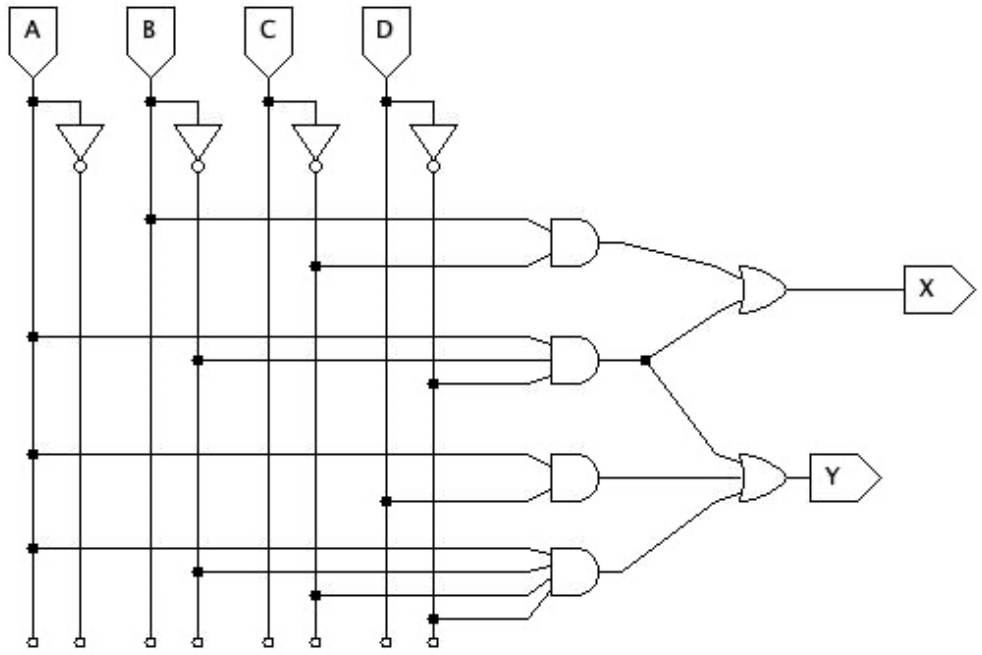
6. Implement the below with only NAND gates (it's the same function in 5). Sketch the circuit or use JLS to create the circuit diagram:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

7. Write the Boolean equations for the circuit below (no need to minimize: give the exact equations implemented in the circuit):



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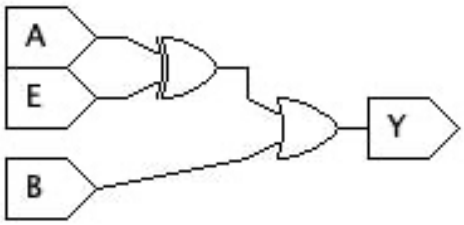
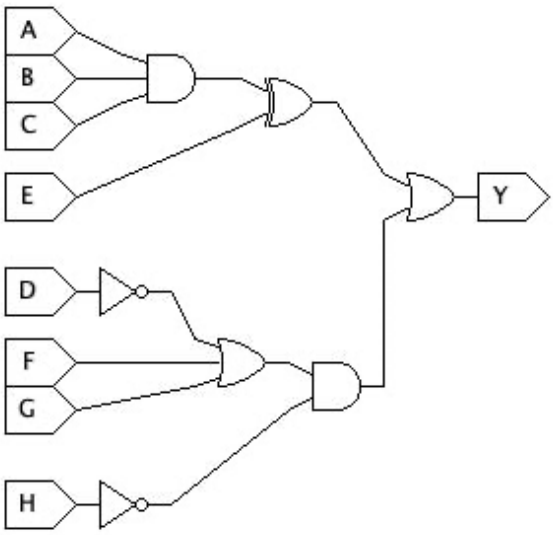
For the next four problems assume the propagation delays are:

Gate	t_{pd} (ps)
NOT	15
2-input NAND	20
3-input NAND	30
4-input NAND	45
2-input NOR	30
3-input NOR	45
2-input AND	30
3-input AND	40
4-input AND	50
2-input OR	40
3-input OR	55
4-input OR	70
2-input XOR	60

8. Determine the propagation delay of:



9. Determine the propagation delay of:



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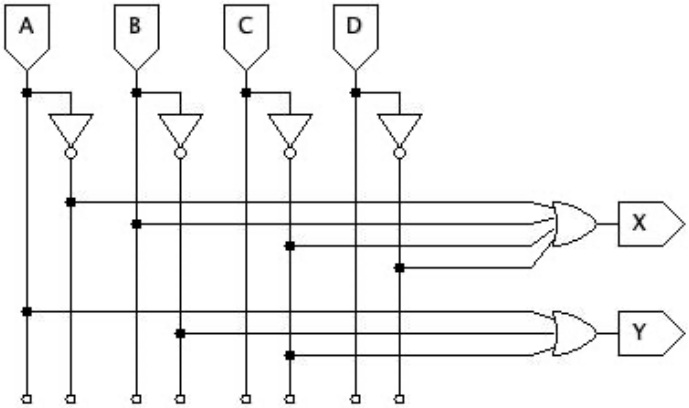
10. Determine the propagation delay of:



11. ERROR: No problem 11 (is/was redundant with 9; Now removed)

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12.1 Consider adding 2-digit binary numbers, A and B, to produce the 2-bit result, S, and a carry-out, C:

$$\begin{array}{rcc} & A_1 & A_0 \\ + & B_1 & B_0 \\ C & S_1 & S_0 \end{array}$$

Develop the truth table and sum-of-products equations for adding the two, 2-bit numbers and produce the 3-bits of the result.

12.2 ***Download the JLS starter file from the assignment page*** and complete the circuit. Note that it uses 2-bit inputs for A and B. You test all possible combinations of inputs to confirm your 2-bit adder works correctly. Hints:

- Think carefully about the structure of the truth table and the terms being used for each output.
- Some product terms can be reused for different outputs.
- JLS has parts called "named wires". Named wires can be used to organize your work and re-use common terms. Named wires have two parts: the source ("name a wire" is shown when you hover over the named wire part on the menu) and connections ("connect to a named wire"). You can use more than one of the "connect to a named wire" part to have a single wire connect multiple places without having a literal wire (line) running across the diagram. If you use named wires, try to name them with a name that describes their purpose.
- Some wires and parts have already been provided. They are intended to provide one tidy approach to laying out the circuit.
- This circuit uses multi-bit inputs and separates them into their individual bits (A0, A1, etc.) for you. Test signal values can be specified in decimal rather than binary. For example, A can be 0, 1, 2, or 3. When A is 2 its individual bits, A1 and A0, are 1 and 0 respectively. The bits of S are combined into a single, 2-bit output, which doesn't include C.
- Carefully think about test cases. A signal generator has already been provided.
- ***DO NOT change the names of either input or output ports.*** The Autograder depends on them being named as-is.

13. JLS problem: **See assignment page and use the provided starter file!**